Low Cost 10-Bit Monolithic D/A Converter

AD561

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/aerospace is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD561

2.0 Part Number. The complete part number(s) of this specification follow:

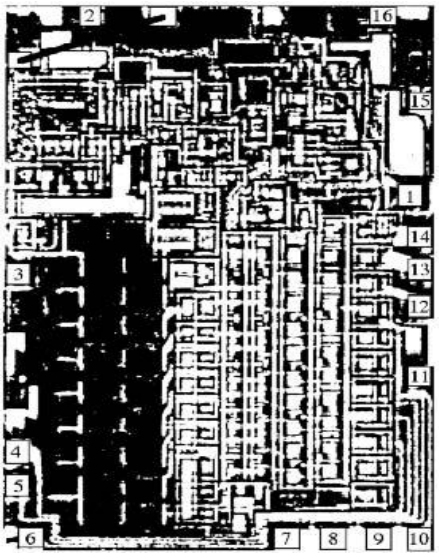
Part Number	Description
AD561-000C	Low Cost 10-Bit Monolithic D/A Converter

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
106 mil x 153 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1. GND
2. BPOS
3. -Vs
4. LSB
5. BIT 9
6. BIT 8
7. BIT 7
8. BIT 6
9. BIT 5
10. BIT 4
11. BIT 3
12. BIT 2
13. MSB
14. +Vs
15. I_{OUT}
16. RFB

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3.3 Absolute Maximum Ratings 1/ 2/

Digital Input Voltage (V_{IN})	V_{CC} to Ground
Output Voltage Compliance (V_{OUT})	-2V to +10V
10V Span Resistor to Ground	V_{CC} to V_{EE}
Bipolar Offset Resistor To Ground	V_{CC} to V_{EE}
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Supply Voltage	±16.5V
Junction Temperature (T_J)	175°C

Absolute Maximum Ratings Notes

1/ T_A = 25°C, unless otherwise noted.
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Sample Size and Qual Acceptance Criteria – 25/2
(b) Qual Sample Package – Sidebrazed DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Relative Accuracy	RA			±0.5	LSB
Differential Nonlinearity	DNL	Major carry transitions		±1	LSB
Gain Error 2/	A_E	With fixed 25Ω resistor		±0.5	% of FS
Unipolar Offset Error 2/	V_{OS}			±0.05	% of FS
Bipolar Zero Error	B_{PZE}	With 10Ω resistor		±3.5	LSB
Output Current	I_{OUT}	Digital inputs at logic "1"	1.5	2.4	mA
Power Supply Gain Sensitivity	P_{SS1}	V_{CC}, +4.5V to +5.5V V_{CC}, +13.5V to +16.5V		±10	PPM of FS/%
	P_{SS2}	V_{EE}, -10.8V to -13.2V V_{EE}, -13.2V to -16.5V		±25	

Table I - Dice Electrical Characteristics (continued)					
Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Power Supply Current 2/	I_{CC}	V_{CC}, +4.5V to +16.5V		10	mA
	I_{EE}	V_{EE}, -10.8V to -16.5V		16	
Power Dissipation	P_D			500	mW
Digital Input High Voltage	V_{IH}		2.0		V
Digital Input Low Voltage	V_{IL}			0.8	V
Digital Input High Current	I_{IH}	Digital "1" = 15V		±100	nA
Digital Input Low Current	I_{IL}	Digital "0" = 0V		±25	µA

Table I Notes:

1/ V_{CC} = +5V, V_{EE} = -15V, T_A = 25°C, unless otherwise specified.
2/ Also tested in CMOS mode. V_{CC} = +15V, V_{EE} = -15V, V_{IH} = 10.5V, V_{IL} = 4.5V.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Relative Accuracy	RA		1		±0.5	LSB
Differential Nonlinearity	DNL	Major carry transitions	1, 2, 3		±1	LSB
Gain Error 2/	A_E	With fixed 25Ω resistor	1		±0.5	% of FS
Gain Error Temperature Coefficient	TCA_E		2, 3		±60	ppm of FS/°C
Unipolar Offset Error 2/	V_{OS}		1		±0.05	% of FS
Unipolar Error Temperature Coefficient	TCV_{OS}		2, 3		±10	ppm of FS/°C
Bipolar Zero Error	B_{PZE}	With 10Ω resistor	1		±3.5	LSB
Bipolar Zero Error Temperature Coefficient	TCB_{PZE}		2, 3		±20	ppm of FS/°C
Output Current	I_{OUT}	Digital inputs at logic "1"	1	1.5	2.4	mA
Power Supply Gain Sensitivity	P_{SS1}	V_{CC}, +4.5V to +5.5V V_{CC}, +13.5V to +16.5V	1		±10	PPM of FS/%
	P_{SS2}	V_{EE}, -10.8V to -13.2V V_{EE}, -13.2V to -16.5V			±25	
Power Supply Current 2/	I_{CC}	V_{CC}, +4.5V to +16.5V	1		10	mA
	I_{EE}	V_{EE}, -10.8V to -16.5V			16	
Power Dissipation	P_D		1		500	mW
Digital Input High Voltage	V_{IH}		1	2.0		V
Digital Input Low Voltage	V_{IL}		1		0.8	V
Digital Input High Current	I_{IH}	Digital "1" = 15V	1		±100	nA
Digital Input Low Current	I_{IL}	Digital "0" = 0V	1		±25	µA

Table II Notes:

1/ V_{CC} = +5V, V_{EE} = -15V, unless otherwise specified.
2/ Also tested in CMOS mode. V_{CC} = +15V, V_{EE} = -15V, V_{IH} = 10.5V, V_{IL} = 4.5V.

Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table II with the following exceptions)								
Parameter	Symbol	Sub-groups	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
			Min	Max	Min	Max		
Power Supply Current	I_{CC}	1		10		13	±3	mA
	I_{EE}	1		16		19		
Output Current	I_{OUT}	1	1.5	2.4	1.4	2.5	±5	mA

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	4-Nov-111
B	Update web address	Jan. 25, 2002
C	Update web address. Change IOUT delta from 5 to 0.5.	Aug. 14, 2003
D	Update header/footer and add to 1.0 Scope description.	Feb. 26, 2008
E	Add Junction Temperature (T_J)….175°C to 3.3 Absolute Max. Ratings	March 28, 2008
F	Updated Section 4.0c note to indicated pre-screen temp testing being performed.	June 6 2009
G	Updated Fonts and Sizes to ADI Standards	22-Sept-2011

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